



Part Number = DA80000FB20

Compal confidential

Schematics Document

Mobile Penryn ULV singal/dual
core with Intel
Cantiga_GS45/GS40 +ICH9-M SFF
core logic

ULV core logic board

2009-07-23

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A

B

C

D

E

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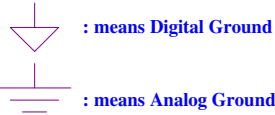
4

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				Block Diagram	

Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.
45@ : means install after SMT.

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

	Descrebtion		Descrebtion		Descrebtion
USB port 0	USB connector	PCI-e port 0		SATA port 0	SATA HDD
USB port 1	BT Module	PCI-e port 1	WLAN Conn.	SATA port 1	
USB port 2	cardreader	PCI-e port 2		SATA port 2	WWAN/SSD
USB port 3	USB connector	PCI-e port 3			
USB port 4	WLAN Conn.	PCI-e port 4			
USB port 5	WWAN/SSD	PCI-e port 5	LAN		
USB port 6	USB connector				
USB port 7	CMOS				
USB port 8	Fingerprint				

I2C / SMBUS ADDRESSING

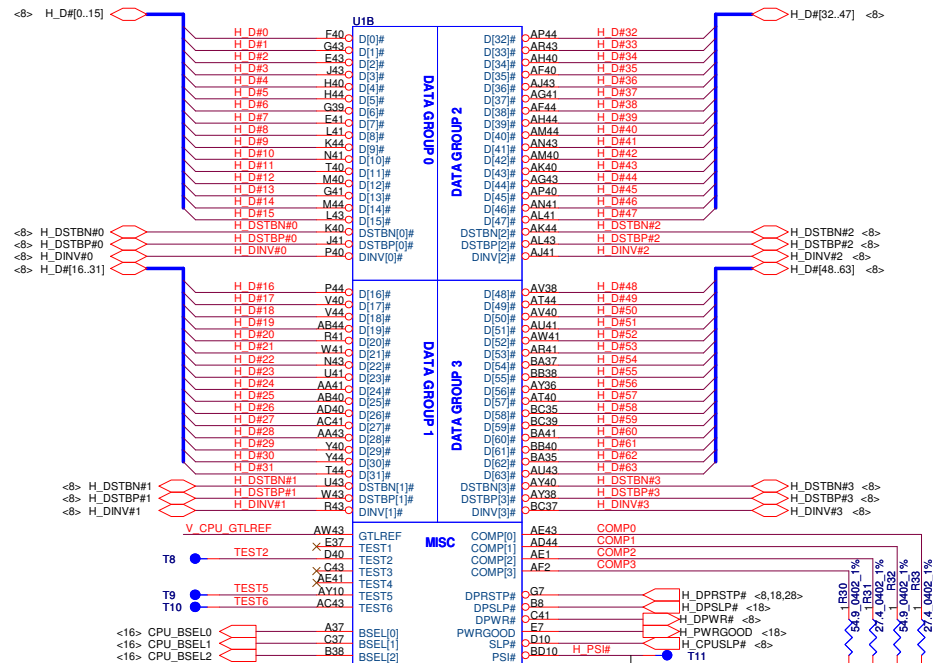
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

Rev
3

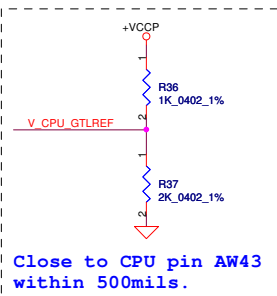


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

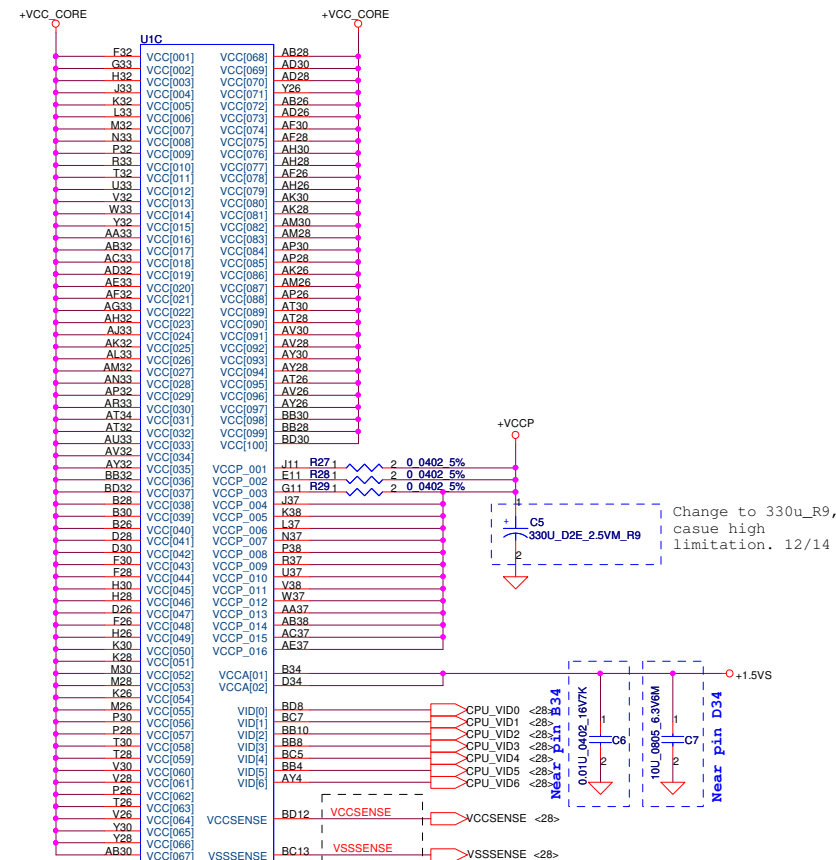
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

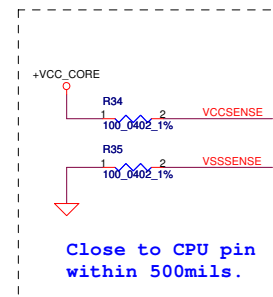
Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02



Close to CPU pin AW43 within 500mils.



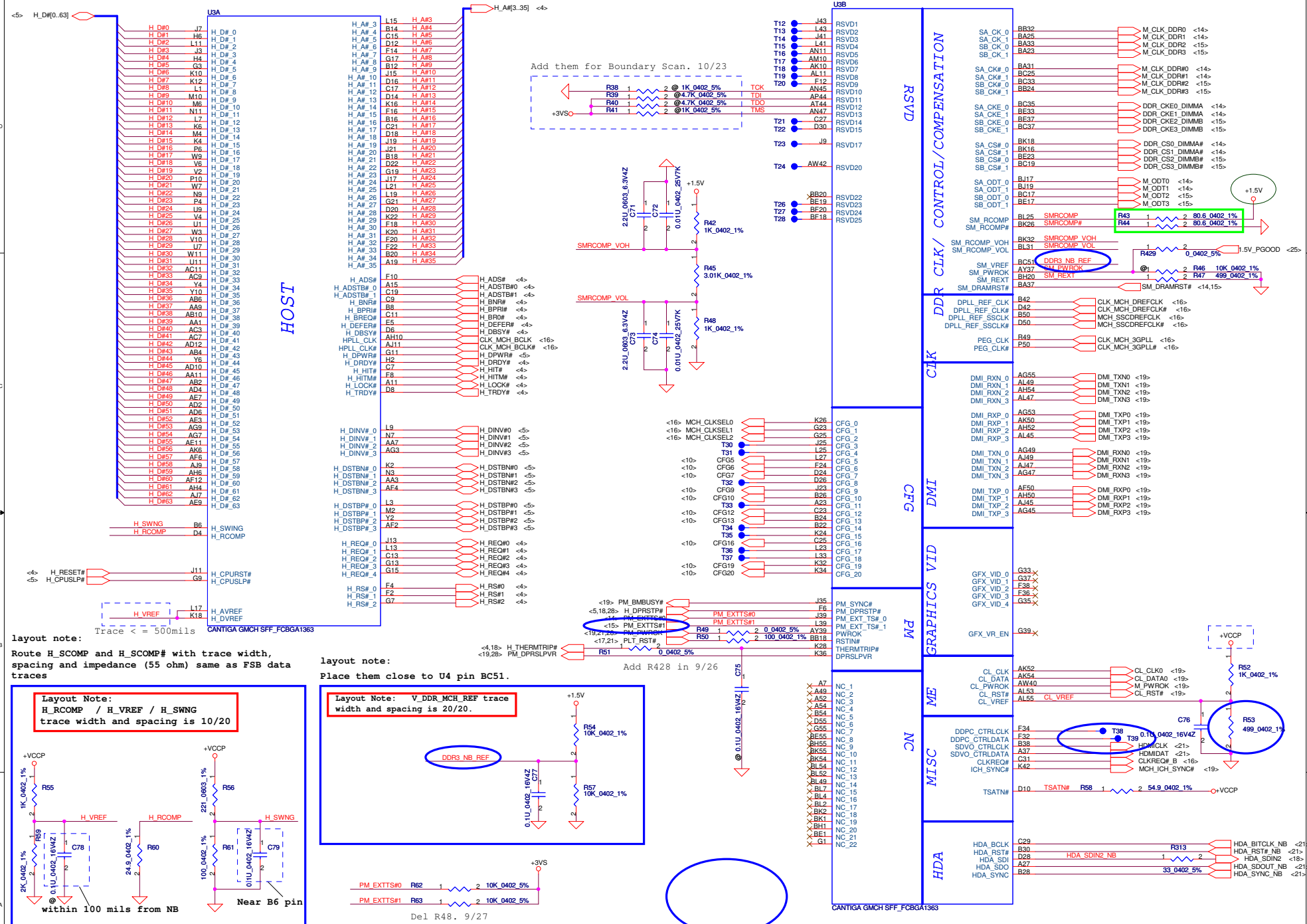
Length match within 25 mils. The trace width/space/other is 20/7/25.

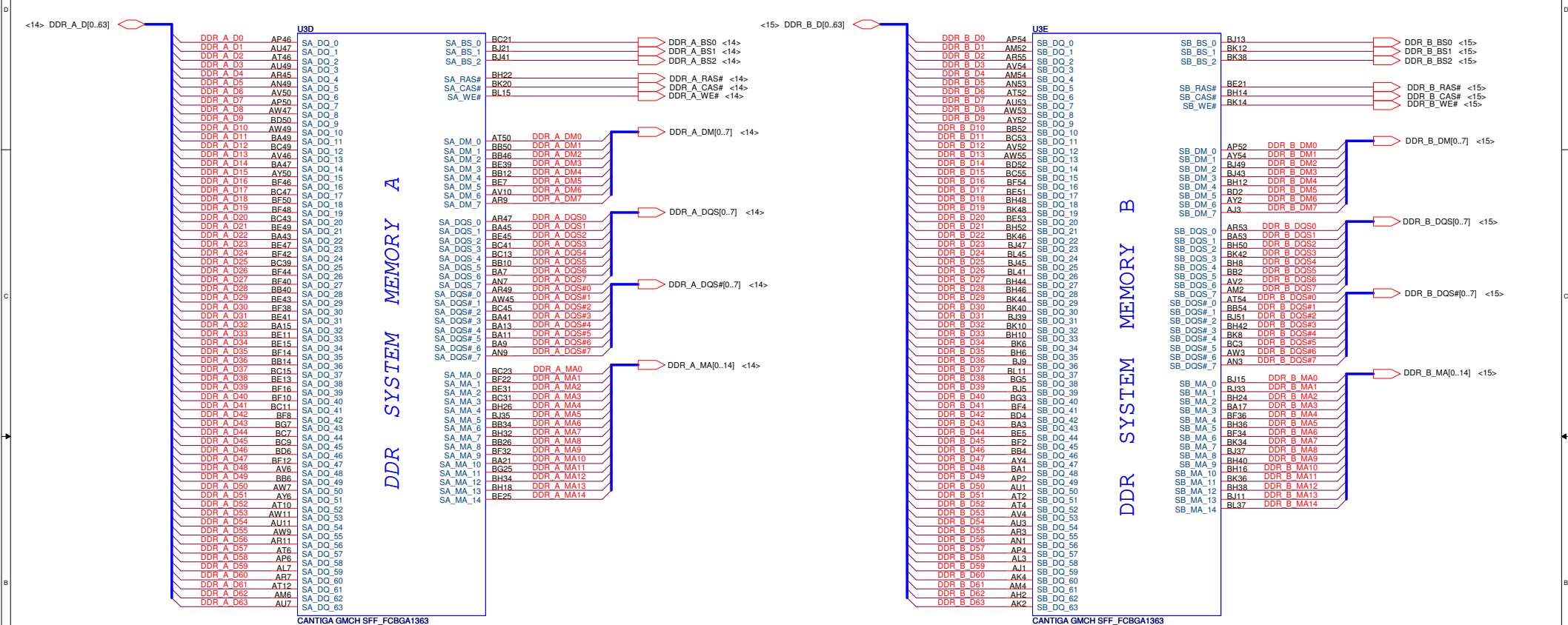


Close to CPU pin within 500mils.

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CANTIGA GMCH SFF_FCBGA1363

CANTIGA GMCH SFF_FCBGA1363

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				Cantiga(2/6)-DDR2 A/B CH		
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VSS

VSS NCTF

755 608

VSS_NCTF_1
VSS_NCTF_2
VSS_NCTF_3
VSS_NCTF_4
VSS_NCTF_5
VSS_NCTF_6
VSS_NCTF_7
VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
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VSS_NCTF_22
VSS_NCTF_23

VSS_SCB_1
VSS_SCB_2
VSS_SCB_3
VSS_SCB_4
VSS_SCB_5
VSS_SCB_6
VSS_SCB_7

CANTIGA GMCH SFF_FCBGA1363

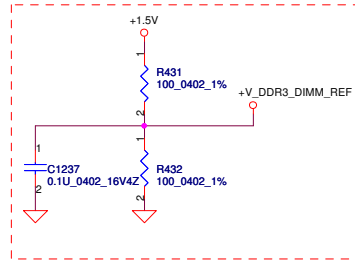
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Cantiga(6/6)-PWR/GND

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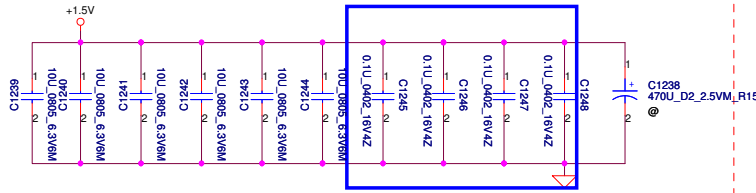
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<9> DDR_A_DQS#[0..7]
 <9> DDR_A_D[0..63]
 <9> DDR_A_DM[0..7]
 <9> DDR_A_DQS[0..7]
 <9> DDR_A_MA[0..14]
 <9> DDR_A_BS[0..2]

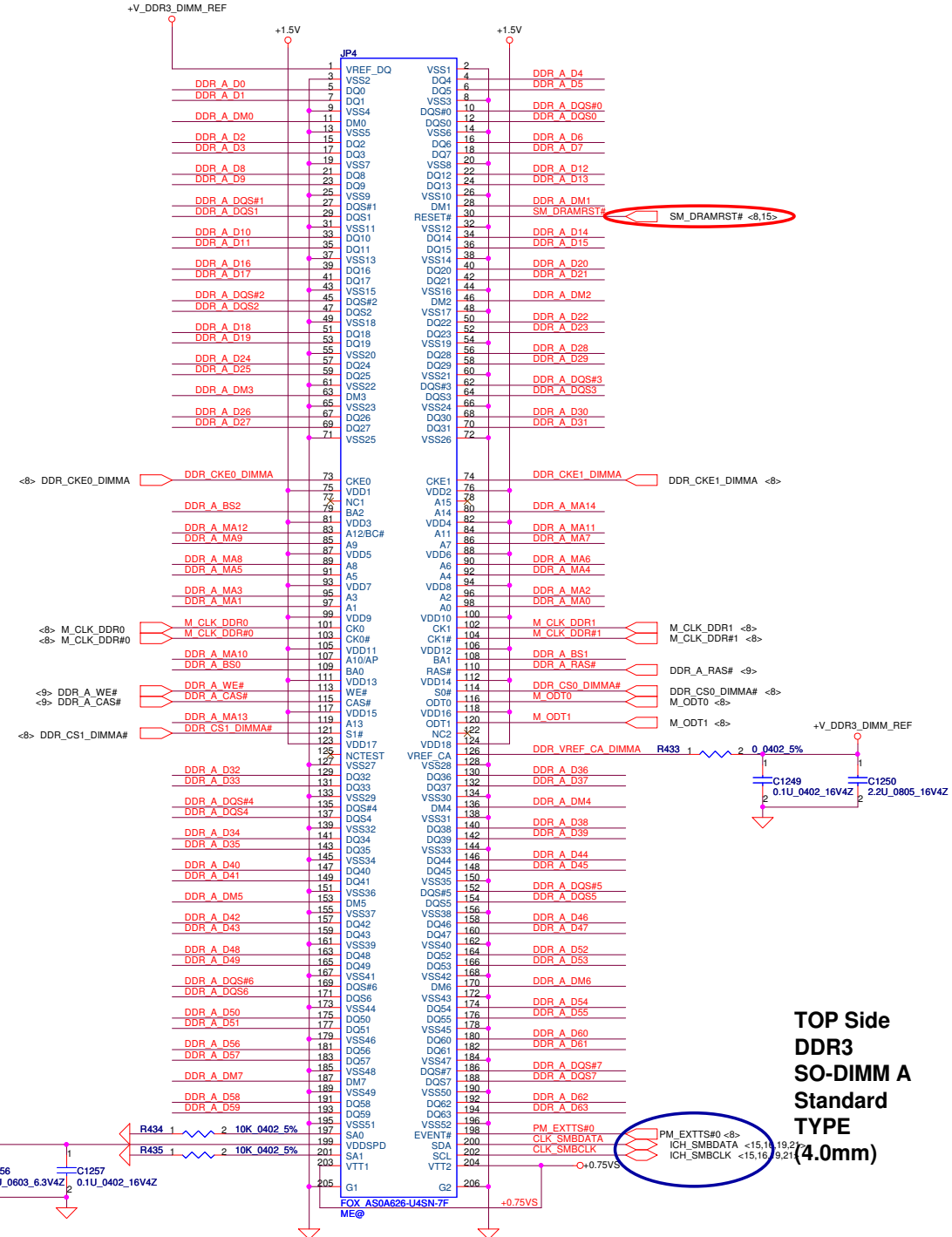
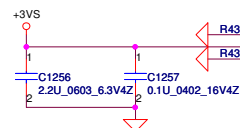
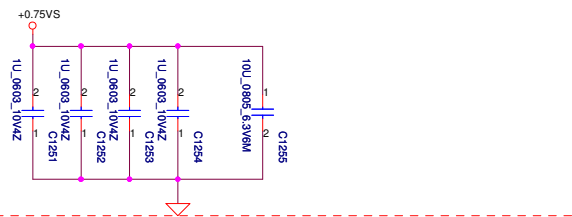


Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

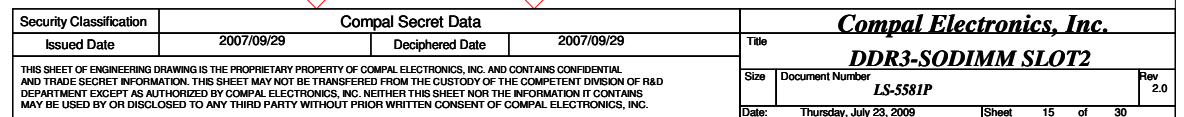


Layout Note:
Place near JP3.203 & JP3.204

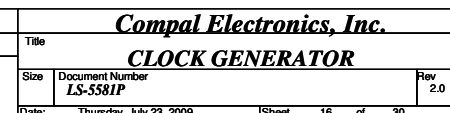
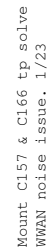


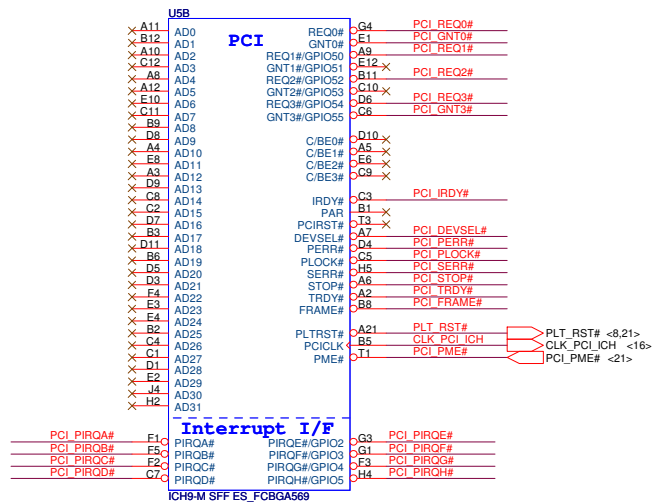
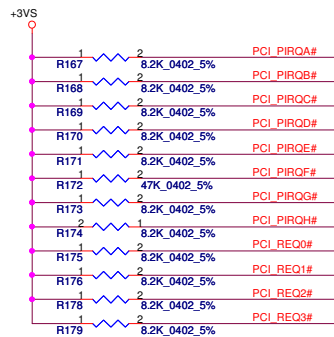
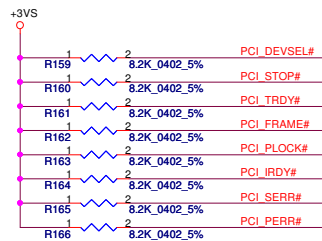
**TOP Side
DDR3
SO-DIMM A
Standard
TYPE
(4.0mm)**

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				Custmr							
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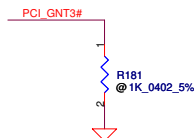


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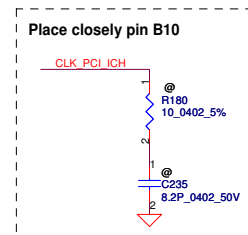
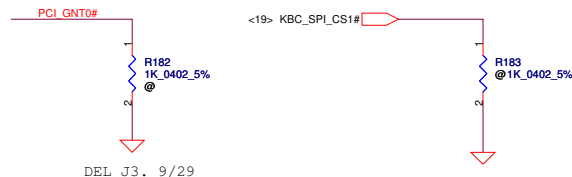


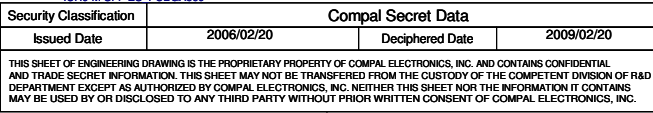


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



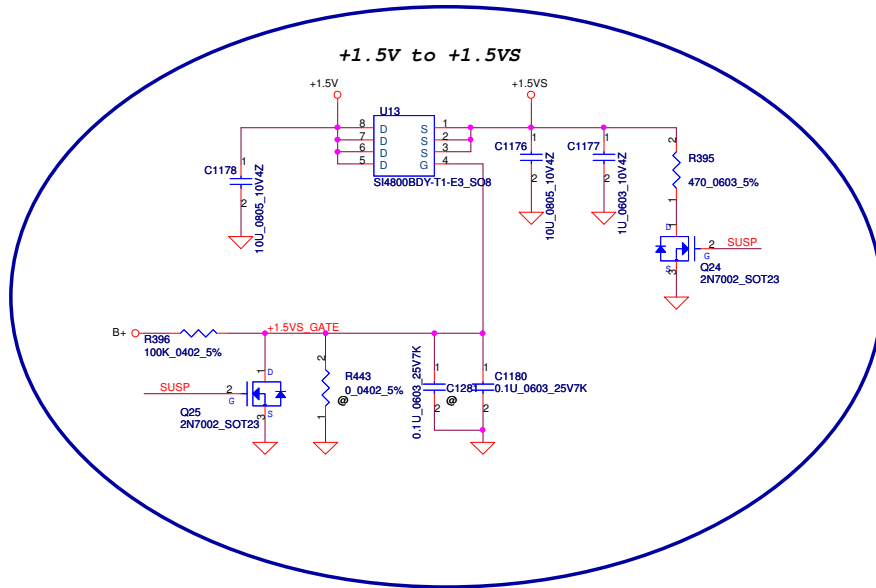
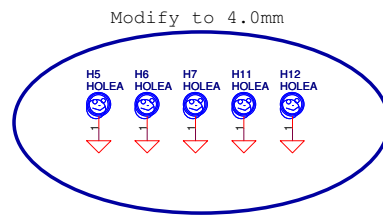
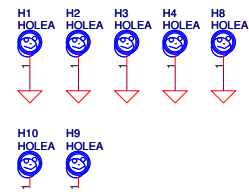
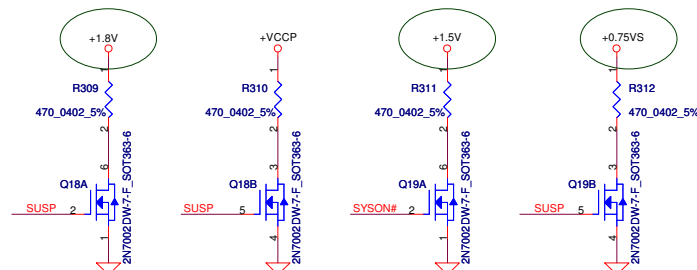
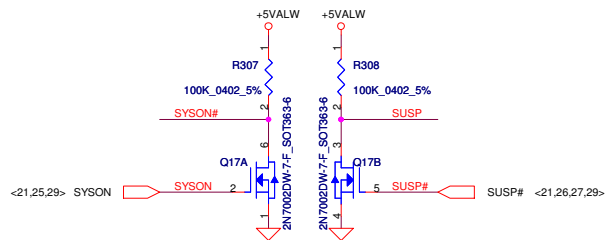
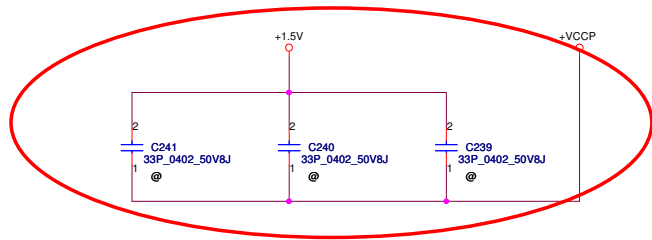
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





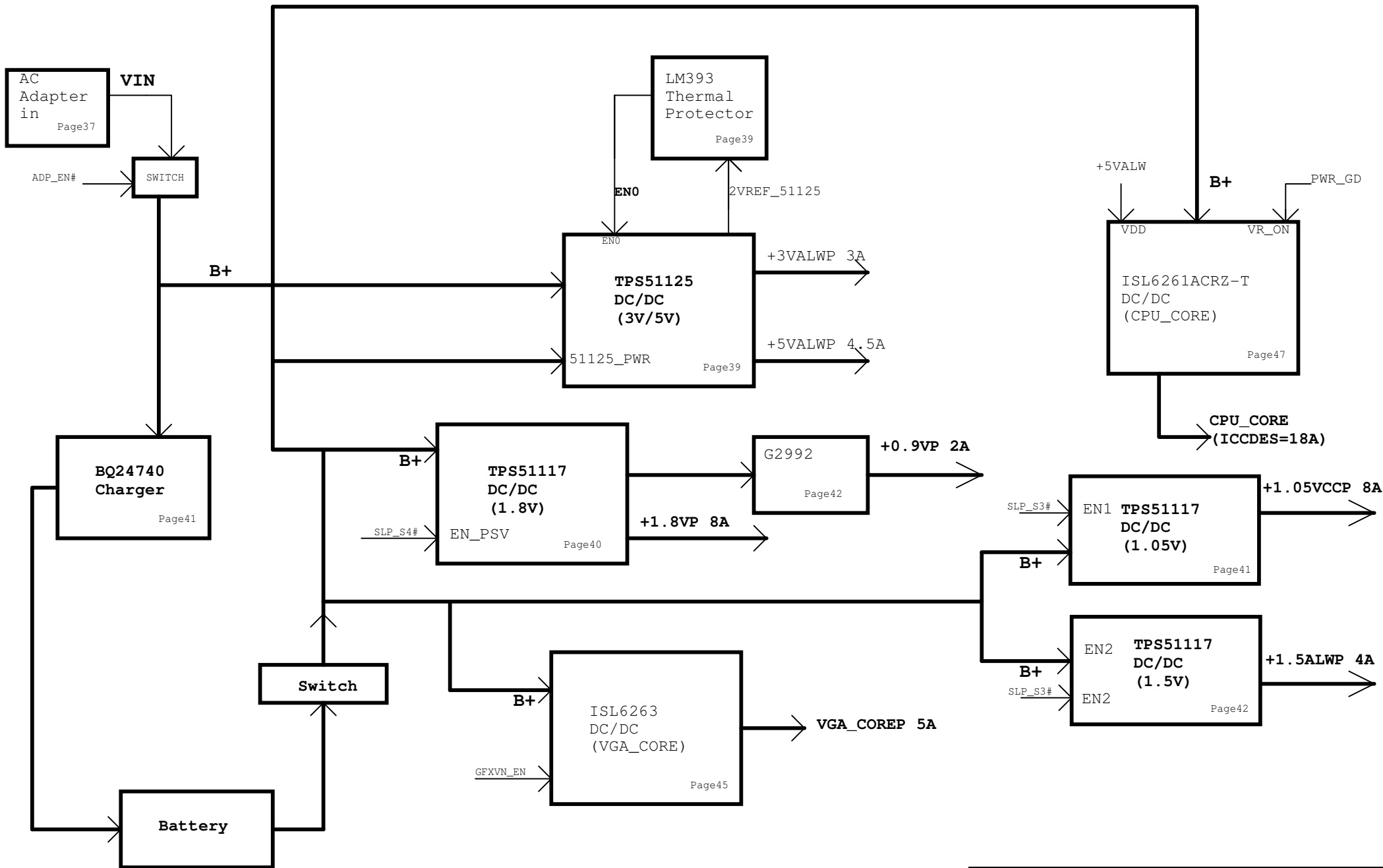


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Title			
ICH9(4/4) POWER&GND			
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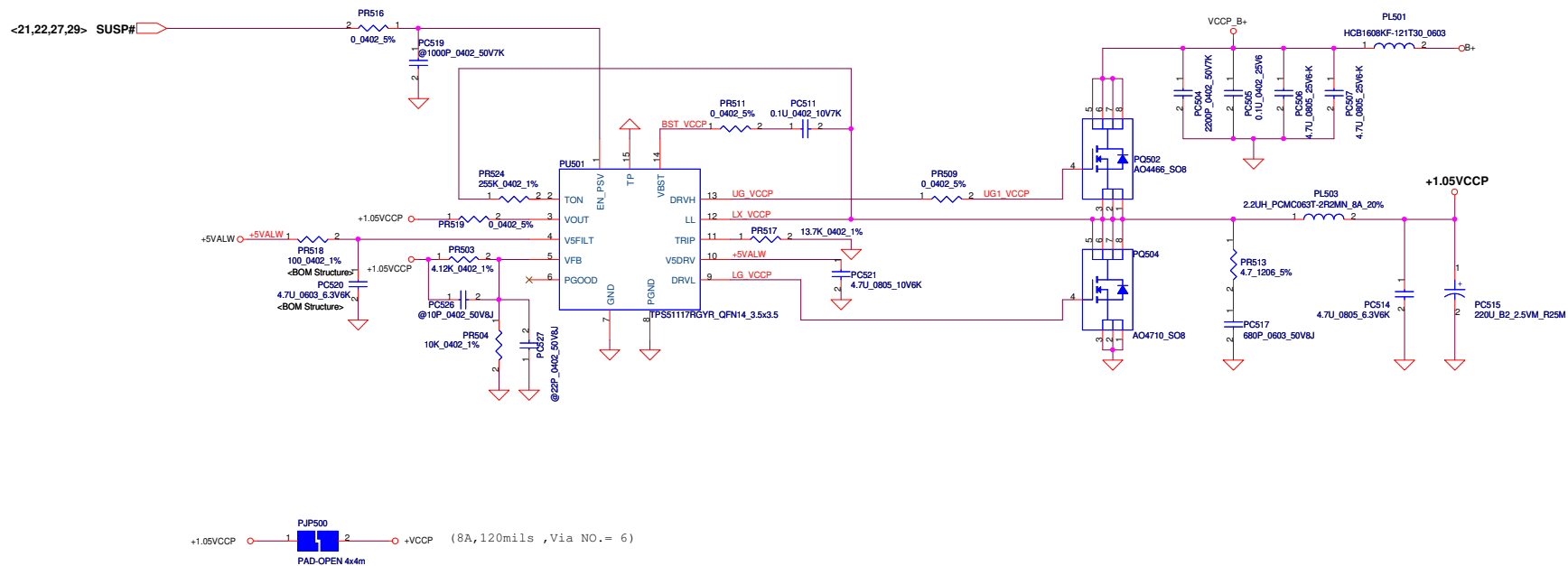


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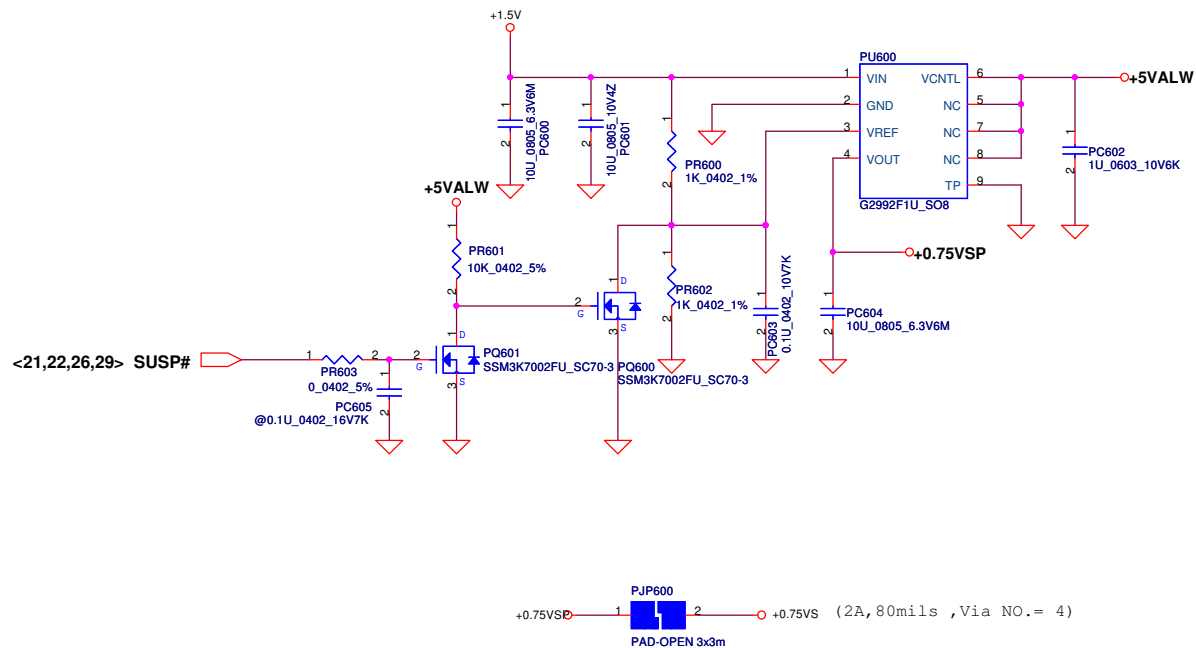
Date	Descreibung	Rev.
4/16	Relaese LS5581PR01 schematic.	01
5/8	<div>R53 change to 499 Ohm</div> <div>R68,R69,R70 implement 75Ohm</div> <div>Add C1303 for DDR3 request</div> <div>Change R149,R177 from 33 to 15Ohm</div> <div>Change C233,C234 from 33P to 22P</div> <div>R153 implement 10K Ohm and R156 remove</div> <div>Add C1079,C1080 for EMI</div> <div>Delete R249,R255,R267,R268 for optionUSB and GPIO</div> <div>Delete C1066,C1067,C1068,C1069,C1070,C1071 for SATA AC cap</div> <div>Add VL voltage on JP6.6 for OCP use</div> <div>Modify SB VCCSUSHDA power level</div> <div>Modify SB GLAN fromPCIE4 to PCIE1</div> <div>Delete R265,C264,C266 for CL_REF1</div> <div>Delete R240 for H_STP_CPU# and Add R444 for H_STP_PCI#</div> <div>Change R221 connect from VGATE to PM_PWRON</div> <div>Change R240 from H_STP_CPU# to H_STP_PCI#</div> <div>Change EC_SCI# from GPIO7 to GPIO12</div> <div>Delete T56,T57,T58,R263 for no use</div> <div>Add R281,R282 for USB OC# pull high</div> <div>Add R242,R285 for Project ID define</div> <div>Modify H5,H6,H7,H11,H12 footprint for ME recommand</div> <div>Delete R251 and Add Q26,D13,R453-R457 for RSMRST# function</div> <div>Delete USB9 pair on SB for not use</div> <div>Modify CLK_PCI_EC from U4.15 to U4.13</div> <div>Modify power plane from +1.8VS to +1.8V for NB use</div> <div>Change Name from DDR3_DIMM_REF to DDR3_NB_REF for DDR3 recommand</div> <div>Change DDRPM_EXTIS# 1 from not use to JP3</div> <div>Del R106 for Intel Recommand for HDMI setting</div>	



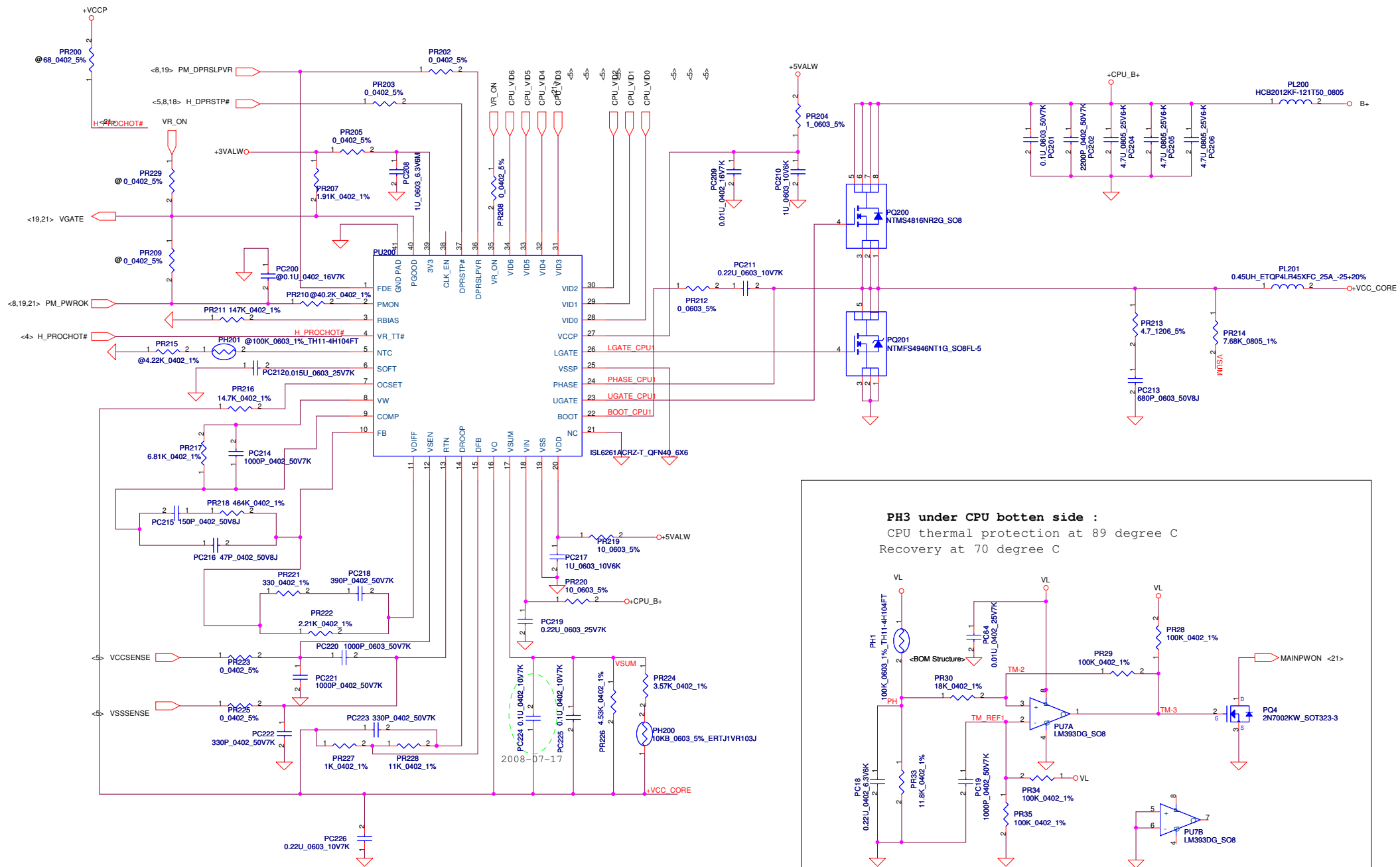
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POWER BLOCK DIAGRAM		
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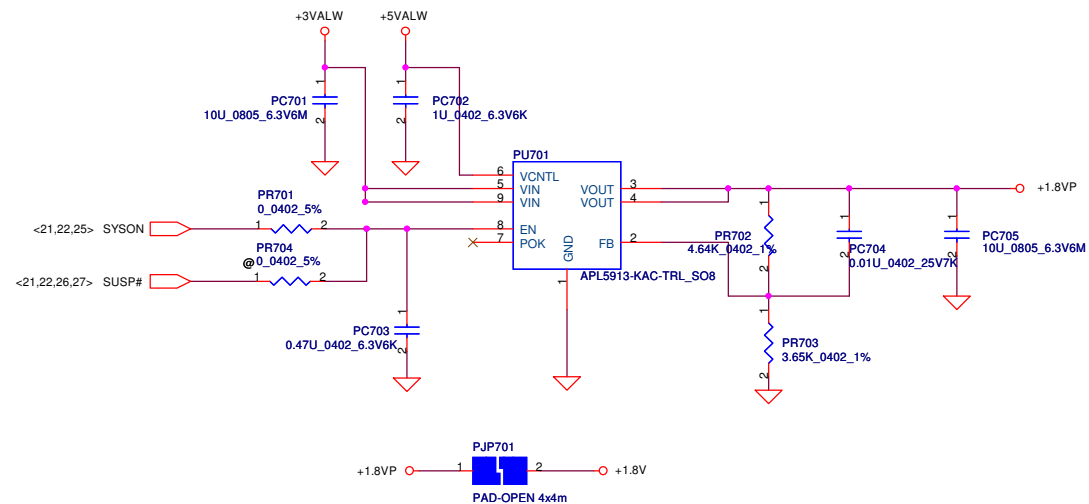
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Item	Reason for change	PG#	Modify List	Date	Phase
1	change OTP 89 degree protect 70 degree recover	B	change PR33=11.8k PR30=18k PR29=100k PR28=100K		
2	Change 1.8vp sequence to SYSON	B	Del PR704		
3	Change 1.5vp Voltage set for hw request	B	change PR407 to 10.5K		
4	For solve RT8209 issue	B	change PR405 PR518 to 100 PC406 PC520 to 4.7U		
5	modify PQ600 PQ601 PN follow C38 bom	C	modify 2N7002 from Rohm to toshiba		
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	GM VGA CORE
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